Electronic Version
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Claims

[c1] What is claimed is:

1.A method of forming a flash memory comprising:

providing a substrate having a first conductive type shallow doped region;

forming at least a stacked gate structure, the stacked gate structure from bottom to top comprising a tunneling oxide, a floating gate, an insulating layer, and a control gate;

performing a first ion implantation process to form a first conductive type deep doped region in the substrate alongside the stacked gate structure;

performing an oxidization process to oxidize an edge part of the floating gate and the control gate for forming an insulating barrier layer having a rounded shape, and for driving in dopants of the deep doped region;

performing a second ion implantation process to form two second conductive type doped regions, which respectively serve as a drain and a source of the flash memory, in the substrate alongside the stacked gate structure; and

forming a bit line contact and a bit line, the bit line being electrically connected to the drain and the deep doped

region through the bit line contact.

[c2] 2.The method of claim 1 wherein the substrate further comprises a second conductive type well, and the shallow doped region, the deep doped region, the drain, and the source are positioned above the second conductive type well.

[c3] 3.The method of claim 2 wherein the first conductive type is P type and the second conductive type is N type.

[c4] 4.The method of claim 1 wherein the control gate further comprises a silicide layer thereon.

[c5] 5.The method of claim 1 wherein the stacked gate structure further comprises a TEOS layer thereon.

[c6] 6.The method of claim 1 wherein the insulating barrier layer is an oxide layer, and the oxidization process is performed at a temperature ranging from 800°C to 1000°C.

[c7] 7.The method of claim 1 wherein the insulating barrier layer is a composite-layer structure comprising at least an oxide layer and at least a nitride layer.

[c8] 8.The method of claim 7 wherein the nitride layer is formed by a rapid thermal nitridation (RTN) process.

[c9] 9.The method of claim 1 wherein the insulating layer is an ONO (oxide-nitride-oxide) layer.

[c10] 10.The method of claim 1 wherein after the drain and the source are formed, the method further comprises:
forming a spacer alongside the stacked gate structure; and
forming an inter-layer dielectric, which covers the stacked gate structure and the spacer, on the substrate.

[c11] 11.The method of claim 1 wherein the flash memory is a BiNOR flash memory.

[c12] 12.A flash memory cell comprising:
a substrate;
a stacked gate structure positioned on the substrate, wherein the stacked gate structure from bottom to top comprises a tunneling oxide, a floating gate, an insulating layer, and a control gate, the floating gate and the control gate having an insulating barrier layer with rounded edges;
a first conductive type shallow doped region positioned in the substrate under the stacked gate structure;
a first conductive type deep region positioned in the substrate at one side of the stacked gate structure;
a second conductive type drain doped region positioned in the substrate at a same side with the deep doped re-

gion, a bottom and sidewalls of the drain doped region being surrounded by the deep doped region; and a second conductive type source doped region positioned in the substrate at an opposite side of the stacked gate structure.

[c13] 13.The flash memory cell of claim 12 wherein the substrate further comprises a second conductive type well, and the shallow doped region, the deep doped region, the drain doped region, and the source doped region are positioned above the second conductive type well.

[c14] 14.The flash memory cell of claim 12 wherein the first conductive type is P type and the second conductive type is N type.

[c15] 15.The flash memory cell of claim 12 wherein the control gate further comprises a silicide layer thereon.

[c16] 16.The flash memory cell of claim 12 wherein the stacked gate structure further comprises a TEOS layer thereon.

[c17] 17.The flash memory cell of claim 12 wherein the insulating layer is an oxide layer.

[c18] 18.The flash memory cell of claim 12 wherein the insulating barrier layer composite-layer structure comprises

at least an oxide layer and at least a nitride layer.

[c19] 19.The flash memory cell of claim 12 wherein the insulating layer is an ONO (oxide-nitride-oxide) layer.

[c20] 20.The flash memory cell of claim 12 wherein the drain doped region and the deep doped region are electrically connected together.